FIRST-ARTICLE ASSEMBLY GUIDE

BLADE-INFRA-OT

IT/OT Bridge Governance Appliance - Prototype Build Procedure

Companion to:	**ICD-INFRA-OT-001 Rev. A**
Build target:	**First-article prototype, single unit**
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Hardware source:	**Blueprint.am (3E8 Robotics) export, May 2026**
BOM:	**47 line items, ~US$6,288 bare parts / ~US$14,410 typical config**
Distribution:	**Public release under CC BY 4.0**

Purpose. This guide provides the complete, step-by-step procedure to assemble one first-article BLADE-INFRA-OT prototype from the Blueprint hardware specification. It covers fabrication of mechanical parts, wiring of the two compute planes and power tree, power-on bring-up, and final enclosure. Step content is derived directly from the Blueprint electrical connection graph (35 edges), mechanical connection graph (42 fixings), and the 47-line bill of materials.

Safety and status. This is a research prototype build at TRL 2–3. Mains-voltage wiring is involved; perform AC work only with the unit unplugged and verified de-energized. The completed unit has not undergone formal first-article test or safety certification.

Tools required

- 3D printer (PETG / ABS for structural, transparent PLA for light pipes), high-temperature filament for the governance heatsink block
- ESD-safe workstation: grounded mat, wrist strap, ionizer if available
- Soldering station with fine tip (for RJ-45 thru-hole and point-of-load passives), hot-air rework optional
- Hex key set: M2, M2.5, M3, M4; torque driver with 0.3–2.5 N·m range
- Precision screwdrivers (M2 / M2.5), thread-locking compound (medium strength)
- Wire strippers, ferrule crimper, ratcheting RJ-45 / DB-9 hand tools
- Digital multimeter (DC volts, continuity, insulation if available)
- Thermal adhesive applicator and thermal interface material (gap pad + paste)
- Conformal coating spray or brush, masking for connectors
- Bench DC supply (24 V) and isolated AC source with current limiting for bring-up

Assumptions

- Access to high-temperature filament and an enclosed printer for the governance heatsink riser
- Familiarity with high-speed signal integrity (10G SFP+, GbE) handling and ESD discipline
- A provisioning environment for the TPM 2.0 (Infineon SLB 9670) and the secure element (Microchip ATECC608B)
- Familiarity with IPMI / BMC (ASPEED AST2500) firmware configuration
- The two custom PCBs (network motherboard, governance mezzanine) have been fabricated 4-layer ENIG and bare-board electrical-tested

1 Fabrication

Fabricate and prepare all mechanical parts before any electronics are handled. Print at high infill (≥ 40%) for structural parts; the governance heatsink riser must be printed in high-temperature filament because it sits in the thermal path of the Kria K26 SOM.

1.1 Print high-temp thermal blocks and component mounts

Print the governance heatsink block and the network heatsink block. These couple the Kria K26 and the Intel Atom SBC respectively to the chassis extrusion. Use high-temperature filament (or, preferably, substitute a machined copper-infused block for the governance side, which carries the higher steady-state load). Print the component mount adapters for the managed switch (M2.5 standoffs), TPM, secure element, IPMI BMC, alarm relay, and the two SFP+ cages.

- Governance heatsink block - high-temp / copper-infused, couples to chassis top cover
- Network heatsink block - thermal spreader to extruded aluminum surface
- Switch / TPM / secure-element / BMC / relay / 2× SFP+ mount adapters (M2–M3 hole patterns)

> **CHECKPOINT.** Verify each mount's hole pattern matches its part's datasheet bolt circle before proceeding. Dry-fit each board onto its adapter.

1.2 Print front-panel interface and light-pipe array

Print the three front-bezel LED mounts (power, AUTHREX-armed, alarm) and the transparent light-pipe array that channels light from the PCB-mounted Dialight LEDs to the bezel face. Print in transparent PLA so the pipes transmit cleanly. The LED mounts snap-fit to the bezel; the light pipes press-fit with an interference fit.

> **CHECKPOINT.** Hold each printed light pipe to a bright source and confirm even transmission with no layer-line scatter; reprint at finer layer height if cloudy.

1.3 Print power-supply and secondary component mounts

Print the PSU retainer bracket that secures the TDK-Lambda CUS100ME AC/DC module in the rear-left chassis bay, and the front-panel light-pipe retainers. Confirm the retainer clears the AC inlet and the 24 VDC terminal block routing.

1.4 Prepare 1U chassis with threaded inserts and EMI gaskets

Take the Penn Elcom 1U extruded-aluminum chassis. Install M3 threaded inserts at all PCB-standoff, divider, heatsink, and bracket locations per the mechanical layout. Apply the Laird EMI fingerstock gasket to the front bezel mating edge using its pressure-sensitive adhesive. Install the Schurter IEC C14 locking clip (snap-fit) at the AC inlet aperture.

- M3 threaded inserts: PCB standoffs, EMI divider standoffs, heatsink bolts, PSU bracket
- Laird EMI fingerstock → front bezel (PSA), beryllium-copper, for EMC seal
- Schurter 4700.0001 IEC C14 locking clip (snap-fit) at AC inlet

> **CHECKPOINT.** Test-fit the steel EMI divider into its standoffs; it must seat flat and bond electrically to the chassis (measure < 0.1 Ω chassis-to-divider).

1.5 Drill and tap mounting holes for DIN-rail adapter

For the DIN-rail variant only: drill and tap the chassis side wall for the M4 side-mount bolts that secure the 1U-to-DIN-rail L-brackets. Deburr and touch up the powder coat. Skip this step for the rack-mount-only variant.

2 Wiring

All electronics handling is ESD-controlled. Populate and wire the network motherboard first (it carries the packet path and power tree), then the governance mezzanine. Follow the Blueprint electrical connection graph; the power tree and signal-bus assignments below are taken directly from it.

2.1 Solder RJ-45 jacks and magnetics to network motherboard

Solder the four Amphenol RJ-45 jacks (IT-IN, OT-OUT, IT-MON, OT-MON) to the network motherboard as thru-hole parts. Place the Bourns quad GbE magnetics between the Marvell 88E6390X switch and the jacks. Per the connection graph, the switch drives the magnetics (data ×4), which fan out to IT-IN and OT-OUT (the inline bump-in-the-wire pair) and to IT-MON and OT-MON (the read-only mirror taps). Maintain controlled-impedance routing for all GbE pairs.

- switch_chip → magnetics_quad (data ×4)
- magnetics_quad → rj45_it_in, rj45_ot_out (inline path)
- magnetics_quad → rj45_it_mon, rj45_ot_mon (mirror taps)

> **CHECKPOINT.** Continuity-check each pair through the magnetics; verify 1500 VRMS isolation barrier integrity between jack shield and board ground.

2.2 Populate point-of-load buck regulators on power rails

Populate the five point-of-load converters on the network motherboard and governance mezzanine. The 12 V buck (TI LM25085) is fed from the AC/DC supply and is the parent rail; it feeds the governance SOM, the network SBC, and cascades to the 3.3 V buck (TPS5430). The 5 V (TPS5450), 1.8 V (ADI LTC3633), and 1.0 V (LTC7130) rails supply the remaining loads. The 1.8 V and 1.0 V rails are the Kria core supplies and must meet ±3% tolerance.

- ac_power_supply → buck_12v (parent rail)
- buck_12v → governance_som, network_sbc, and → buck_3v3 (cascade)
- buck_5v → governance_som; buck_3v3 → governance_som (3.3 V logic + status LEDs)
- buck_1v8 → governance_som (Kria core, ±3%); buck_1v0 → governance_som (Kria core, ±3%)

> **CHECKPOINT.** Before connecting any compute module, power the boards from the bench supply and verify every rail in sequence: 12.0 V, 5.0 V, 3.3 V, 1.8 V, 1.0 V, each within tolerance, with no compute module seated.

2.3 Wire primary AC and secondary DC isolated power inputs

Wire the TDK-Lambda CUS100ME AC/DC module to the IEC C14 inlet (line, neutral, earth). Bond chassis ground to safety earth at the inlet. Wire the Vicor DCM3623 isolated module to the 24 VDC station-service terminal block. Both sources feed the 12 V rail through an OR-ing arrangement for automatic hot-swap. Establish the single star-point signal ground at the inter-plane bus connector.

- dc_dc_isolated → governance_som, network_sbc (secondary power path)
- ac_power_supply → buck_12v (primary power path)
- Chassis ground bonded to safety earth at AC inlet; signal-ground star point at inter-plane bus

> **CHECKPOINT.** With AC only: confirm rails up. With 24 VDC only: confirm rails up. Apply both, then remove each in turn - confirm < 5 ms hand-off with no rail dropout and an alarm log on loss.

2.4 Terminate 40-pin ribbon bus between plane interfaces

Build and terminate the custom shielded 40-way ribbon that carries the inter-plane bus. Per the connection graph, the path is governance_som → ribbon_bus → network_sbc. This is the only data path between the two planes; it is rate-limited and monotonic by firmware. Route the ribbon across the steel divider through its single pass-through, keeping the shield bonded at the governance end only to avoid a ground loop.

> **CHECKPOINT.** Verify the ribbon shield is grounded at one end only. Continuity-check all 40 ways end to end; confirm no shorts to the shield.

2.5 Connect alarm relay and front-panel status LEDs

Wire the TE Connectivity IM03TS Form-C alarm relay to the governance SOM GPIO (fault-trip line). Wire the three Dialight status LEDs to the governance SOM: power (3.3 V indicator), AUTHREX-armed (GPIO), and alarm (GPIO). The TPM connects to the governance SOM over SPI; the secure element over I2C; the IPMI BMC links to the governance SOM over UART (OOB console) and to the network SBC for IPMI monitoring.

- governance_som → alarm_relay (GPIO fault-trip)
- governance_som → status_led_power / status_led_armed / status_led_alarm
- governance_som → tpm_module (SPI, audit security); governance_som → secure_element (I2C, root of trust)
- bmc_controller → governance_som (UART, OOB console); bmc_controller → network_sbc (IPMI monitoring)
- network_sbc → switch_chip (I2C switch management); switch_chip → sfp_cage_1 / sfp_cage_2 (10G fiber)

> **CHECKPOINT.** Bench-toggle each GPIO and confirm the corresponding LED and the relay actuate. Verify the relay's Form-C contacts switch (NO opens, NC closes) on a simulated fault.

3 Bring-up

Bring-up proceeds only after all rail checks in Section 2 pass with no compute modules seated. Seat modules, then power up in the documented order.

3.1 Verify voltage rails and power-on sequencing

Seat the Kria K26 SOM onto the governance mezzanine (240-pin connector) and the Atom SBC onto the network motherboard (board-to-board standoffs). Apply power and verify the power-on sequence: 12 V parent comes up first, then 3.3 V and 5 V logic, then the Kria 1.8 V and 1.0 V core rails last. Confirm the power LED illuminates and no rail collapses under load.

> **CHECKPOINT.** Scope the 1.0 V and 1.8 V Kria core rails for clean sequencing and < 3% ripple under load. Abort if either core rail overshoots.

3.2 Initialize TPM 2.0 and secure element root of trust

Provision the Infineon SLB 9670 TPM and the Microchip ATECC608B secure element. Take ownership of the TPM, generate the endorsement and storage root keys, and provision the audit-ledger Ed25519 signing key into the secure element. Confirm the governance SOM can read the TPM over SPI and the secure element over I2C, and that the SOM can produce a valid signature over a test ledger record.

> **CHECKPOINT.** Generate a test audit-ledger entry, sign it, and verify the Ed25519 signature and the BLAKE3 hash-chain link off-device. Both must validate.

3.3 Configure IPMI BMC and verify sideband management

Flash and configure the ASPEED AST2500 BMC. Set the OOB management IP on the dedicated IPMI port, confirm the serial-over-LAN console reaches the governance SOM over UART, and confirm the BMC can read network-SBC health telemetry. Verify the OOB interface is air-gapped from the data plane - no packets should cross between the IPMI port and the inline/mirror ports.

> **CHECKPOINT.** Run a packet capture on the data plane while exercising the OOB port. Confirm zero leakage between OOB and data planes (verification item V-20).

3.4 Test OT protocol parsing on the inline path and SFP+

Load the protocol parser processes on the Atom SBC. Inject test traffic for each supported protocol - Modbus, DNP3, IEC 61850 MMS/GOOSE/SV, OPC UA, EtherNet/IP, BACnet - through the IT-IN port and confirm the parser emits a correct abstract-syntax-tree to the governance plane over the ribbon bus. Confirm the switch passes traffic on both copper (IT-IN/OT-OUT) and the two SFP+ fiber cages.

> **CHECKPOINT.** Run simulation scenario 01 (nominal) end to end: a Modbus pump-start should PROPAGATE with all eight AUTHREX stages passing and the audit ledger committing the entry.

3.5 Verify fail-modes and fault-relay trigger

Verify the three failure modes. Inject a governance-plane fault and confirm fail-closed: the inline path opens within 50 ms. Enable fail-bypass and confirm the relay restores connectivity within 10 ms. Confirm fail-alarm-only logs degradation while passing traffic. Run scenario 02 (Monterrey attack) and confirm CARA isolation drops the burst and the tier collapses to T0, with the alarm relay tripping and the alarm LED illuminating.

> **CHECKPOINT.** Scenario 02 must end with the compromised host isolated, the tier at T0, the alarm relay tripped, and a complete forensic ledger preserved (verification item V-14).

4 Assembly

Final mechanical assembly is performed only after bring-up passes. Torque all fasteners to spec and apply conformal coating before final closure.

4.1 Install EMI divider and mount PCBs to standoffs

Install the steel EMI divider on its M3 internal standoffs. Mount the network motherboard to the chassis extrusion on M3 standoffs (bottom bay) and the governance mezzanine to the EMI divider on M3 standoffs (upper bay). Mount the managed switch on its M2.5 standoffs, the TPM and secure element on M2 screws to the divider, the BMC on M3 standoffs to the divider, the alarm relay on M3 screws, and both SFP+ cages on M2 screws to the chassis.

- pcb_network_motherboard → chassis (M3 standoffs); pcb_governance_mezzanine → EMI divider (M3 standoffs)
- switch (M2.5), TPM + secure element (M2), BMC (M3), alarm relay (M3), 2× SFP+ cages (M2)

> **CHECKPOINT.** Torque all standoffs to spec (M2: 0.3 N·m, M2.5: 0.45 N·m, M3: 0.6 N·m). Confirm the divider maintains plane separation with the ribbon as the only crossing.

4.2 Apply thermal compound and secure heatsink blocks

Apply thermal interface material to the Kria K26 and Atom packages. Secure the governance heatsink block and the network heatsink block to the chassis extrusion with thermal adhesive and M3 bolts so that both couple their respective compute package to the chassis top cover, which is the primary convective radiator in this fanless design.

> **CHECKPOINT.** After a 30-minute soak at full simulated load, confirm Kria junction stays within its industrial rating and the chassis top cover is the dominant heat path.

4.3 Seat Kria SOM and SBC onto board connectors

Confirm the Kria K26 SOM is fully seated in its 240-pin connector on the governance mezzanine, and the Atom SBC is secured on its board-to-board standoffs on the network motherboard. Verify retention hardware is torqued and the heatsink blocks maintain compression on the thermal interface material.

4.4 Apply conformal coating and install front bezel

Mask all connectors, the SOM/SBC sockets, and the SFP+ cages. Apply conformal coating to both PCBs for humidity and particulate ingress resistance per the industrial environmental envelope. After cure, install the three status LEDs and the light-pipe array into the front bezel (snap-fit and press-fit), then mount the bezel to the chassis with M3 countersunk screws, compressing the EMI fingerstock gasket.

> **CHECKPOINT.** Confirm conformal coating coverage under UV inspection with no bridging across connector pins. Confirm the bezel gasket is evenly compressed for EMC seal.

4.5 Final rack enclosure closure and labeling

Install the DIN-rail brackets (M4 side-mount) if building the DIN-rail variant. Close the chassis top cover, confirming the heatsink blocks make contact. Affix the FRU serial-number plate and the rear-panel port labels (IT-IN, OT-OUT, IT-MON, OT-MON, IPMI, console). Apply the asset and configuration label noting firmware version and the fail-mode setting (default: fail-closed). The unit is now ready for the verification matrix in ICD-INFRA-OT-001 Rev. A, Section 14.

CHECKPOINT. Final QA: confirm all 20 rear/front labels present and legible; confirm fail-mode label matches the configured firmware setting; record the build against the BOM revision.

End of assembly procedure. Proceed to ICD-INFRA-OT-001 Rev. A, Section 14 (Test and Verification), items V-01 through V-20.